AN14558

Low Power Implementation on MCX A153 MCU Series

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Document information

Information	Content
Keywords	AN14558, MCX A153 MCU series, Low power, Power consumption, Wake-up time
Abstract	This application note introduces the power domains, power modes, highlight configurations, wake up, and low power and wakeup optimization of MCXA153 series. It provides different low power and wake up configurations through demo for user reference.

1 Introduction

MCX A153 series MCUs expand the MCX Arm Cortex-M33 product offerings with multiple high-speed connectivities, operating up to 96 MHz, serial peripherals, timers, analog, and low power consumption.

The power-efficient operating modes are as follows:

- 53 µA/MHz in the Active mode
- 0.34 mA in the Sleep mode
- 20.28 µA in the Deep Sleep mode
- 6.5 µA in the Power Down mode
- 394 nA in the Deep Power Down mode

This application note describes the following contents of the MCX A153 series:

- Power domains and power supplies
- Power modes and low power entry
- Power related configurations
- Wake up source and wake up time
- Low power and wake up optimization
- Low power demo

2 Power domains

As shown in Figure 1, the device contains SYSTEM domain, CORE domain, SRAM domain, ANALOG domain, and USB domain. SYSTEM domain is mainly for power management, which contains SPC, HVD/LVD/POR, FRO16K, WUU, and other modules. CORE domain is mainly for digital logic, which contains CM33, NVIC, DMA, FRO192M, LPUART, and other modules. For specific modules contained in each domain, see the Power domain assignments for modules table in the Reference Manual.

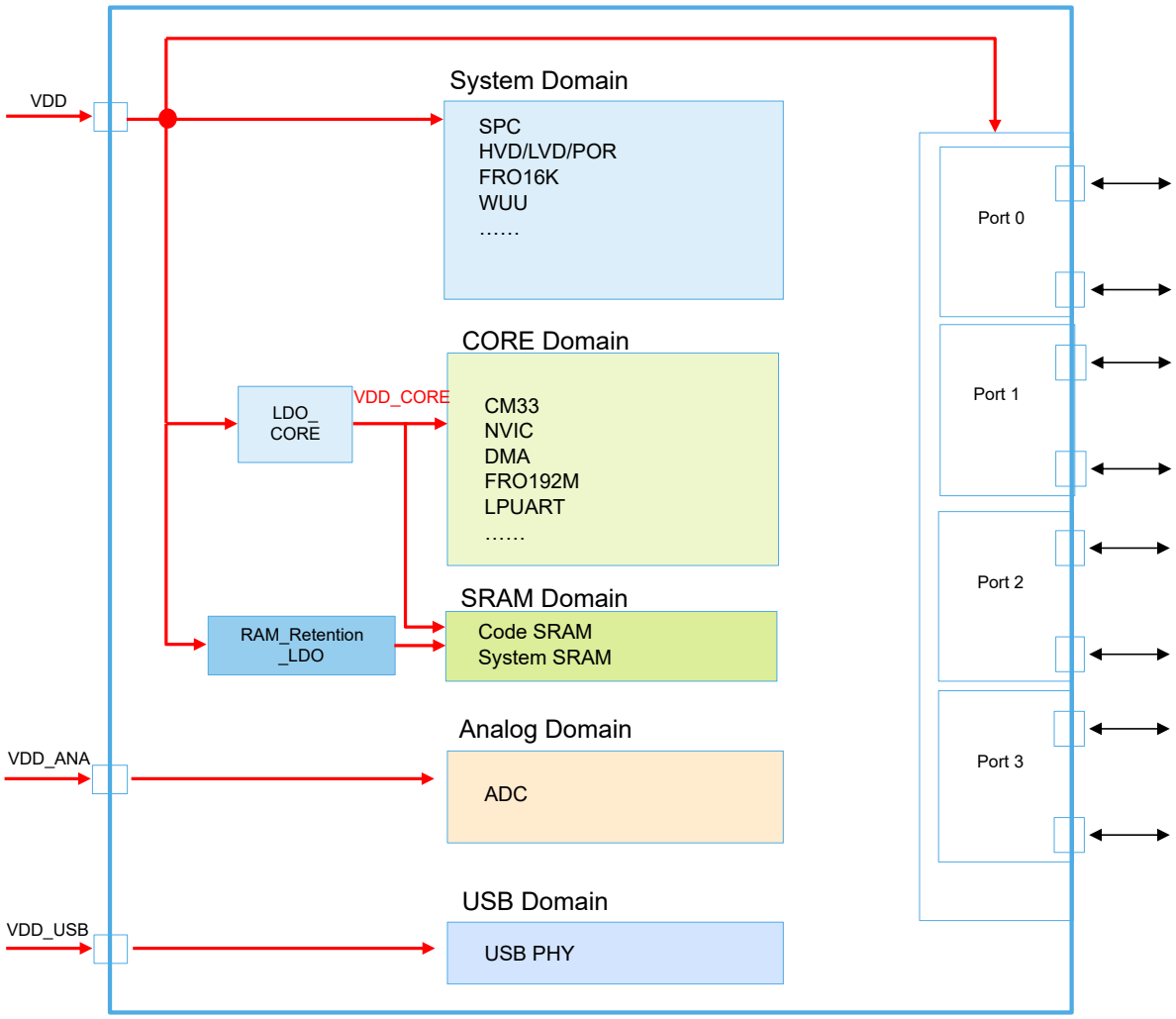

Figure 1. Power domains and power supplies

Table 1 lists the power supply and corresponding voltage range of each power domain. The power supply of the CORE domain is the output voltage `VDD_CORE` of `CORE_LDO`, which is 1.0 V and 1.1 V in active mode and can be a lower voltage in the Power Down mode. When `VDD_CORE` is 1.1 V, the core can reach up to 96 MHz. When `VDD_CORE` is 1.0 V, the core can reach up to 48 MHz. The power supply of the SRAM domain is the output voltage of `CORE_LDO` or `RAM_Retention_LDO`, and `RAM_Retention_LDO` supports SRAM retention switches in the Deep Power Down mode. For the power supply and corresponding voltage range of the remaining power domains, see Table 1.

Table 1. Power supplies and voltage range

Power domain	Power supply	Voltage range
CORE	`LDO_CORE`	Mid voltage (1.0 V), Normal voltage (1.1 V) (Active, Sleep, and Deep Sleep mode)
		Retention voltage (Power Down mode)
		OFF (Deep Power Down mode)
SRAM	`LDO_CORE`	Mid voltage (1.0 V), Normal voltage (1.1 V)

Table 1. Power supplies and voltage range*...continued*

Power domain	Power supply	Voltage range
		(Active and Sleep mode)
	RAM_Retention_LDO	Retention voltage (Deep Sleep, Power Down, and Deep Power Down mode)
SYSTEM	VDD	1.71 – 3.6 V
ANALOG	VDD_ANA	1.61 – 3.7 V
USB	VDD_USB	3.0 – 3.6 V

3 Power modes and low power entry

This section describes power modes and low power entry controllers.

3.1 Power modes

The device supports Active, Sleep, Deep Sleep, Power Down, and Deep Power Down. Table 2 describes the status of Clock, CORE domain, SYSTEM domain, FLASH, SRAM, PORT, and IO in different power modes. You can use Table 2 to compare the status of these modules in different power modes or quickly find the status of these modules in a certain power mode.

Table 2. Modules status and power modes

	CORE domain	CM33	SYSTEM domain	Flash	SRAM	PORT[1]	IO
Active	ON	ON	ON	ON	ON	ON	ON
Sleep	ON	Static[2]	ON	ON	ON	ON	ON
Deep Sleep	Static/LP[3]	Static	ON	Static	Static	Static	ON
Power Down	Static	Static	ON	OFF	Static	Static	Static
Deep Power Down	OFF[4]	OFF	ON	OFF	Static/OFF	OFF	Static

[1] PORT supports pad control functions.
[2] Static means that the module is in the state retention status (no clock but the data can be kept).
[3] LP means can be active with async functional clock.
[4] OFF means power down.

The following sections introduce the features of different power modes.

3.1.1 Active

Default mode after RESET.

- Clocks to CPU, memories, and peripherals are enabled.
- CPU execution is possible.
- Adjust VDD_CORE to the minimum possible value based on the required frequency to achieve optimal power consumption.

3.1.2 Sleep

- The CPU clock is OFF.
- The System and Bus clock remains ON.

- Most modules can remain operational.
- Use the ACTIVE_CFG register to control LDO_CORE voltage level and drive strength.

3.1.3 Deep Sleep

- CPU clock, System clock, and Bus clock are OFF.
- SRAM is in static status (SRAM cannot be accessed, but the data is retained).
- To enable SOSC, SIRC, and FIRC, configure the corresponding STEN bit.
- Some modules can remain operational with low power asynchronous clock sources.

3.1.4 Power Down

It is the lowest power mode that can retain all registers.

- The CPU clock, System clock, and Bus clock are OFF.
- Flash memory is powered off.
- Place the CORE domain of the chip into the static state.
- SRAM is in static status (SRAM cannot be accessed, but the data is retained)
- Configure the SPC LP_CFG[CORELDO_VDD_LVL] to 0000b (retention voltage).

3.1.5 Deep Power Down

The device wakes from the Deep Power Down mode through the Reset routine.

- The CPU clock, System clock, and Bus clock are OFF.
- The Flash memory is powered off.
- The CORE domain is powered off.
- The SYSTEM domain remains ON.
- Support four SRAM retention switches (for details, see On-chip regulators table in SPC chapter for details, and support all SRAM array powered off).

3.2 Low power entry

As shown in Table 5, the power mode entered is controlled by CKCTRL[CKMODE] and PMCTRLMAIN[LPMODE] bitfields.

The CKCTRL[CKMODE] field configures the amount of clock gating when the core enters a low power mode because of WFI or WFE. Table 3 describes the functions corresponding to different CKMODE values. Configuring CKMODE > 0 requires the SLEEPDEEP field in the Arm core to become **1**. Configuring PMCTRLMAIN[LPMODE] > 0 requires writing 1111b to CKMODE.

Table 3. Function of CKMODE field

CKCTRL[CKMODE]	Function
0000b	No clock gating
0001b	Core clock gated
1111b	Core, platform, and peripheral clocks are gated, and the core enters the low power mode.

The PMCTRLMAIN[LPMODE] selects the desired low power mode when a core executes WFI or WFE instruction. If you haven't enabled the protection level using Power Mode Protection (PMPROT), writing to this field is blocked. Table 4 shows the functions corresponding to different LPMODE values.

Table 4. Function of LPMODE field

PMCTRLMAIN[LPMODE]	Function
0000b	Active/Sleep
0001b	Deep Sleep
0011b	Power Down
1111b	Deep Power Down

Table 5 shows all the configurations of the device to enter low power mode.

Table 5. Power mode entry

Power mode	CKCTRL[CKMODE]	PMPROT[LPMODE]	PMCTRLMAIN[LPMODE]
Active	0000b	0000b	0000b
Sleep	0000b	0000b	0000b
	0001b		
Deep Sleep	1111b	0001b	0001b
Power Down	1111b	0011b	0011b
Deep Power Down	1111b	1111b	1111b

4 Power configurations

4.1 Regulator and voltage detectors configurations

Table 6 shows the power-related hardware configurations. ACTIVE_CFG and ACTIVE_CFG1 registers configure the hardware in Active and Sleep mode, such as LDO_CORE voltage level and drive strength. Autonomous change to use LP_CFG and LP_CFG1 when in low power mode (Deep Sleep, Power Down, and Deep Power Down).

Table 6. Power-related hardware configurations

ACTIVE_CFG LP_CFG	**Configures**
	LDO_CORE voltage level
	LDO_CORE drive strength
	Enables
	HVDs, LVDs
	Bandgap, BG buffer
	VDD voltage detect
	Low power current reference IREF
ACTIVE_CFG1 LP_CFG1	**Enables**
	CMPs and CMP DACs
	USB 3 V detect

4.2 Low Power Request (LPREQ) pin

The LPREQ pin asserts after low power entry and negates after low power wake up.

SPC controls the state of the LPREQ pin based on how you configure Low Power Request Configuration (LPREQ_CFG). You control the LPREQ pin in the Active mode. SPC controls the pin when the chip transitions from Active to a Low Power mode, and after wakeup from these Low Power modes.

To use the LPREQ pin:

1. Specify the pin polarity (LPREQ_CFG[LPREQPOL]).
2. Enable the pin output (LPREQ_CFG[LPREQOE]).
3. Configure the pin mux for the desired pin using the PORT PCR registers.

Figure 2 shows the waveform of LPREQ pin, and the explanation of the waveform is listed below:

- CTIMER_MATCH: Hardware toggle IO to indicate the wake up event.
- LPREQ_PIN: LPREQ_CFG[LPREQPOL]=1b, LPREQ_CFG[LPREQOE]=1b, which means that the pin is low after the low power entry and high after wake up.

Figure 2. Waveform of LPREQ pin

4.3 Async DMA

Deep Sleep mode and Power Down mode support use async DMA to partially wake up, and the device automatically re-enters the low power mode after DMA finishes its task.

The following is the introduction to async DMA:

- The async DMA does not require CPU involvement, but does require a Bus clock, which wakes up the MCU from Deep Sleep or Power Down to Sleep mode.
- When the async DMA needs to access the register of a peripheral, enable the Bus clock of the peripheral before entering low power mode by MRCC_GLB_CCx and MRCC_GLB_ACCx registers. When async DMA needs to access SRAM, do not set the SRAM to retention state in Sleep mode.
- When the async DMA is completed, that is, CHx_CSR[DONE] is set, the MCU automatically enters the original low power mode.
- Set CHx_CSR[ERQ] and CHx_CSR[EARQ].
- Table 7 lists all the hardware trig source of async DMA and corresponding slot number. Only modules in LP status not Static status under Deep Sleep or Power Down modes support async DMA. For example, FlexPWM is in Static under Deep Sleep mode, so it cannot support the async DMA.

Table 7. Async DMA configuration

Slot Number	DMA request description	Module name
1	Wake up event	WUU0
11	Receive request	LPI2C0
12	Transmit request	LPI2C0
15	Receive request	LPSPI0
16	Transmit request	LPSPI0
17	Receive request	LPSPI1

Table 7. Async DMA configuration...*continued*

Slot Number	DMA request description	Module name
18	Transmit request	LPSPI1
21	Receive request	LPUART0
22	Transmit request	LPUART0
23	Receive request	LPUART1
24	Transmit request	LPUART1
25	Receive request	LPUART2
26	Transmit request	LPUART2
49	Counter match event	LPTMR0
51	FIFO Request	ADC0
53	DMA_request	CMP0
54	DMA_request	CMP1
60	Pin event request 0	GPIO0
61	Pin event request 0	GPIO1
62	Pin event request 0	GPIO2
63	Pin event request 0	GPIO3

5 Wake up

Table 8 shows normal wake up source and typical wake up time in different low power modes, where the typical wake up time is the data in the datasheet.

Table 8. Wake up information

Symbol	Description	Wake up source	Typical wake up time
tSLEEP	Sleep -> Active	All peripherals	0.21 µs
tDSLEEP	Deep Sleep -> Active	Async peripherals	7.4 µs
tPWDN	Power Down -> Active	WUU, Reset pin	17.1 µs
tDPWDN	Deep Power Down -> Active	WUU, Reset pin	2.36 ms

6 Low power and wake up optimization

This section explains various methods for optimizing power consumption and factors to consider for wake up optimization.

6.1 Power consumption optimization

Following are the different ways of performing power consumption optimization:

- Regulator
  - Configure the appropriate voltage level and drive strength.

  - In the Power Down mode, LDO_CORE can provide retention voltage to the CORE domain.
- Peripherals
  - Disable unused analog peripherals by ACTIVE_CFG1 and LP_CFG1 registers.
- Memories
  - Flash
    - Configure the FLASHCR register to place the Flash memory in the Low Power state.
  - SRAM
    - Auto clock gating by the RAM_CTRL register of SYSCON.
    - SRAM can be individually retained or powered down by software in Deep Power Down mode.
- Clocks
  - Select and configure the appropriate CPU_CLK/SYSTEM_CLK.
  - Disable unused clock source.
  - Configure the MRCC_GLB_CC0/MRCC_GLB_CC1/MRCC_GLB_ACC0/MRCC_GLB_ACC1 to disable or automatic clock gating the clocks to modules.
- Monitors
  - Disable unused voltage monitors (HVDs/LVDs).
- I/O pins
  - For unused I/O pins, use the default configuration (floating input), in which case the leakage current is minimized. With the default configuration, the input buffer and the internal pull resistor are disabled.
  - During the use of I/O pins, reduce the power consumption by appropriately increasing the resistance of the external resistor.

6.2 Wake up time consideration

Here are some points to consider with wake up time:

- SLOW_CLK frequency
  - The wake up process is implemented through CMC. SLOW_CLK is the clock source of CMC and its frequency is equal to ¼ SYSTEM_CLK.
- Different VDD_CORE level
  - Recovery time required for different voltage levels. For details, see the **Low Power Wake up delay** table in the Reference Manual.
- The longer time of clock recovery time and Flash recovery time.
- Interrupt latency.

7 Demo operation

7.1 Hardware requirement

- FRDM-MCXA153 board.
- One Type-C USB cable.

Note:

- *To measure wake up time, prepare an oscilloscope.*
- *To measure power consumption, prepare an MCU-Link Pro or multimeter.*

7.2 Software requirement

- MCUXpresso IDE v11.9.0 or later.
- SDK_2.14.0_FRDM-MCXA153.

7.3 Setup

7.3.1 Hardware connection

Use a Type-C USB cable to connect J15 of FRDM-MCXA153 and the USB port of the personal computer.

7.3.2 Import project

To import a project, perform the following steps:

1. As shown in Figure 3, open MCUXpresso IDE 11.9.0, on the **Quickstart Panel**, choose **Import from Application Code Hub**.

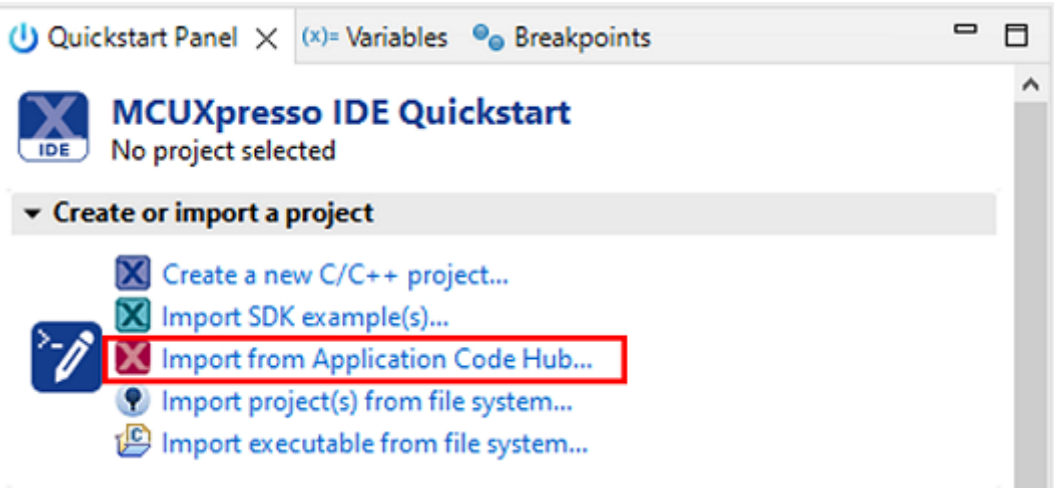

Figure 3. Import from Application Code Hub

2. As shown in Figure 4, enter the **demo name** in the search bar.

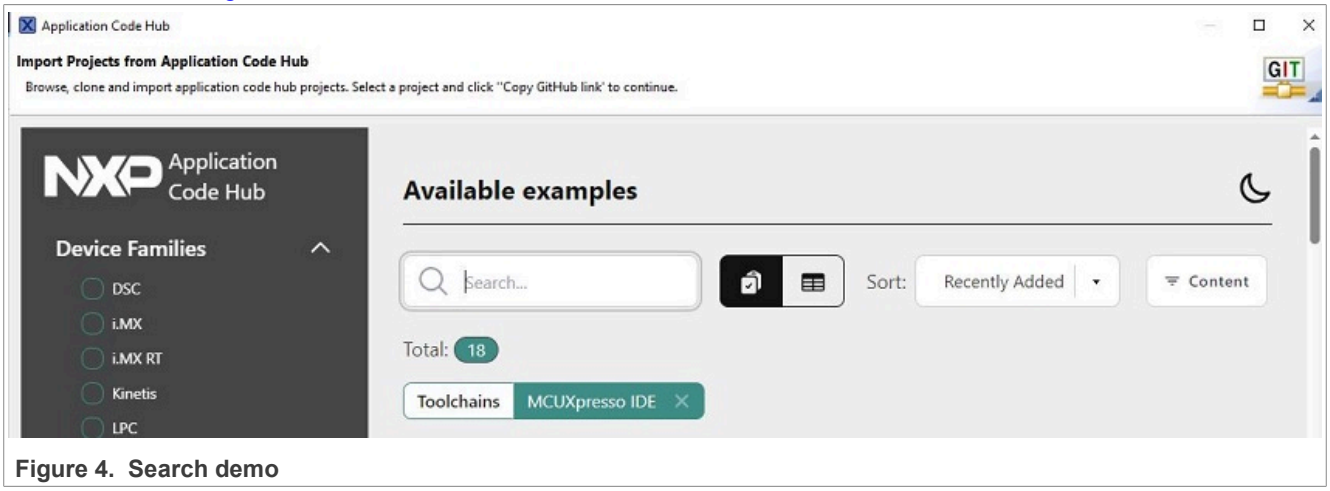

Figure 4. Search demo

3. As shown in Figure 5, click **Copy GitHub link**, MCUXpresso IDE automatically retrieves project attributes, and then click **Next>**.

Figure 5. Copy GitHub link

4. Select the **main** branch, click **Next>**, select the MCUXpresso project, and then click the **Finish** button to complete the import.

Note: *Install the SDK_2.14.0_FRDM-MCXA153 on your MCUXpresso IDE.*

7.3.3 Build and Flash project

To Build and Flash a project, perform the following steps:

1. As shown in Figure 6, click the **Build** button from the toolbar, and then wait for the build to complete.

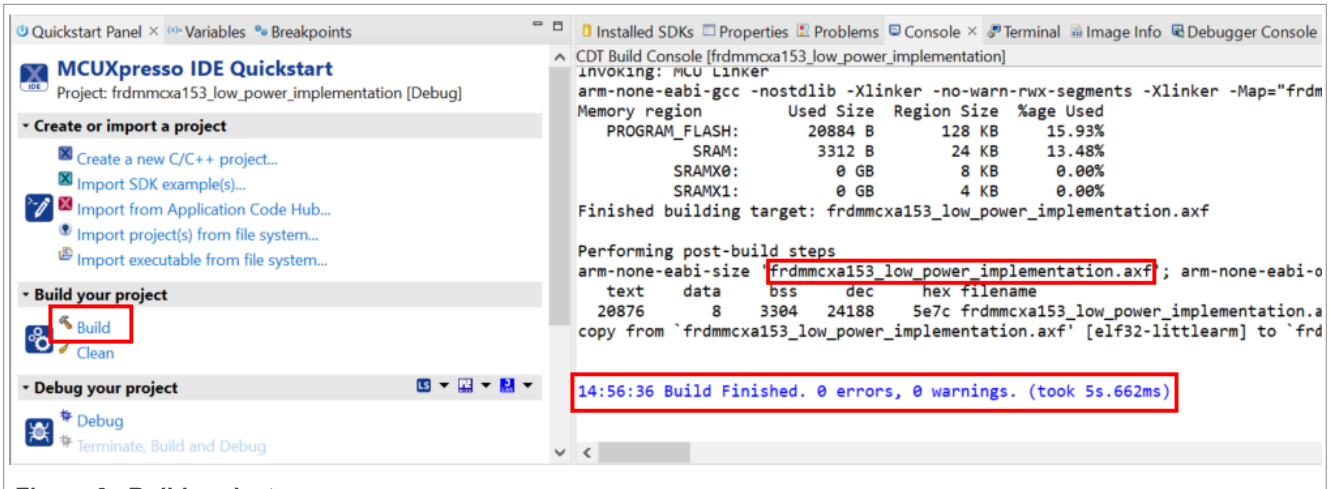

Figure 6. Build project

2. As shown in Figure 7, select the **GUI Flash Tool** from the toolbar to program the executable to the board.

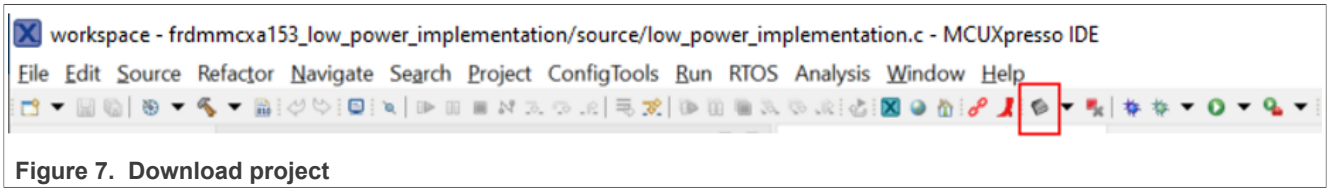

Figure 7. Download project

7.3.4 Select low power mode and wake up configurations

To select the low power mode and wake up configurations, perform the following steps:

1. Open a serial terminal.

2. Follow the prompts in Figure 8. To enter a different Low Power mode, enter one from A to E.

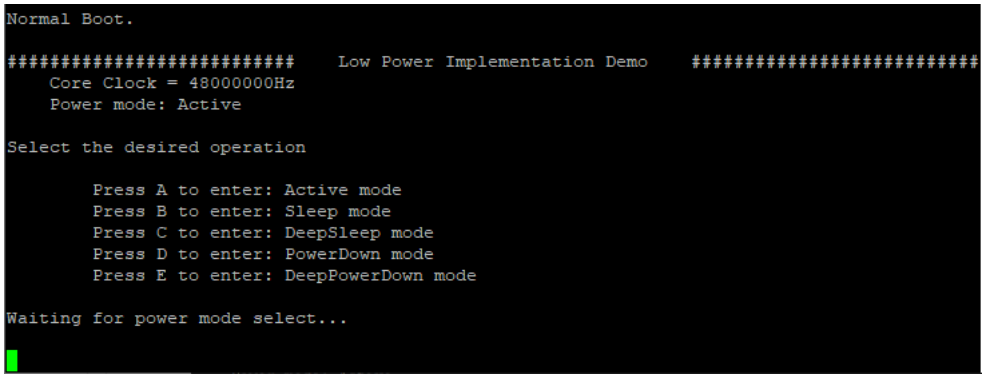

Figure 8. Select low power mode

3. Follow the prompts in Figure 9 and enter one from 1 to 3 to select the wake up mode.
   - The typical wake up mode corresponds to the typical wake up time in the data sheet.
   - The fast wake up mode corresponds to a faster wake up time and often consumes more current.
   - The slow wake up mode corresponds to a slower wake up time and often consumes less current.

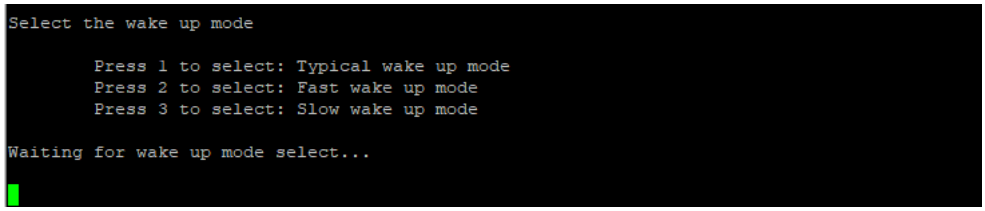

Figure 9. Select wake up mode

4. Figure 10 prompts the selected low power mode and wake up mode, the corresponding wake up time and power consumption, and press SW3 on FRDM-MCXA153 to wake up the MCU.
   Note:
   Press the wake up button when a prompt message appears, otherwise it results in failure to wake up!

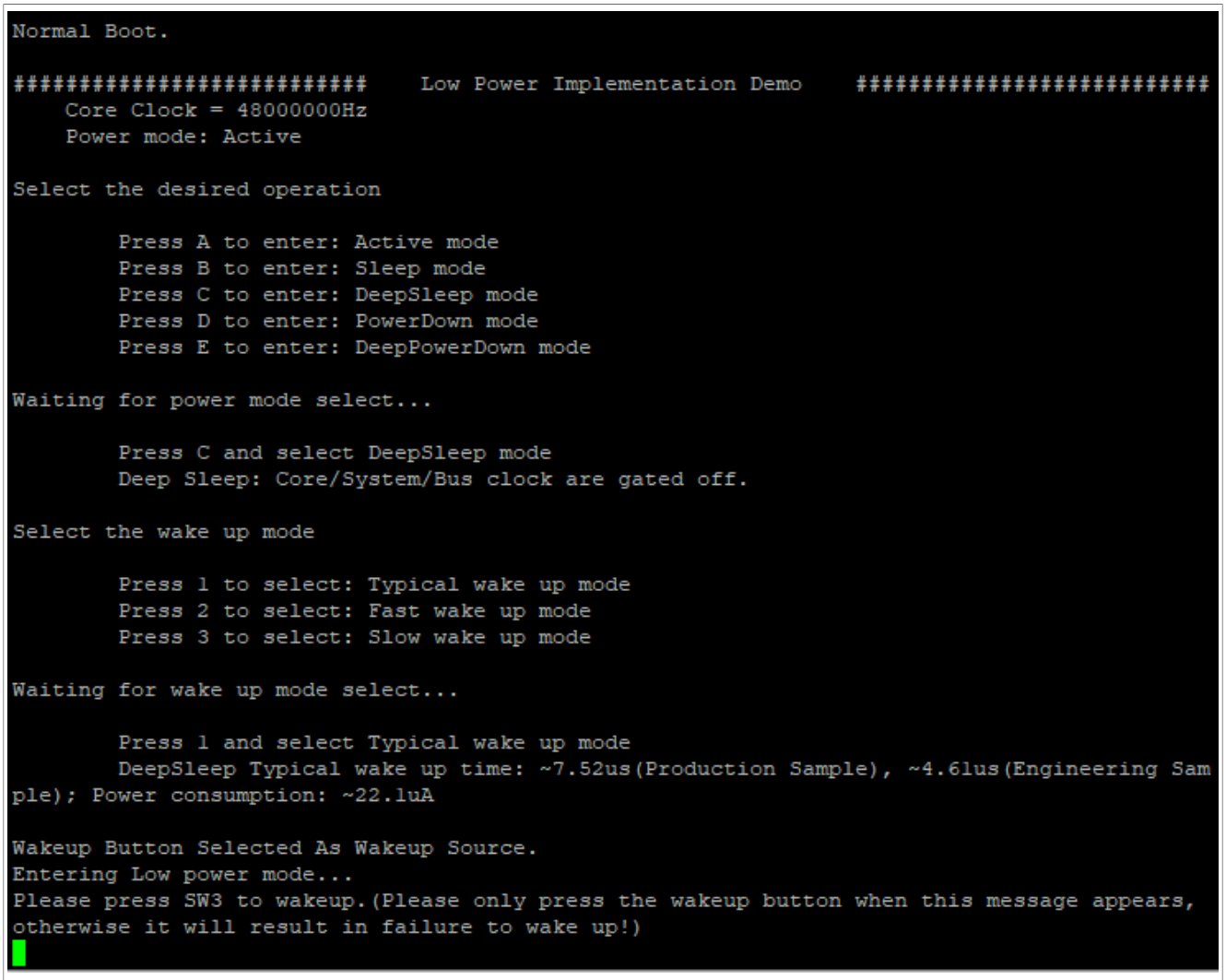

Figure 10. All prompts

7.3.5 Measure power consumption

7.3.5.1 Use MCU-Link Pro and MCUXpresso IDE to measure power consumption

To Use MCU-Link Pro and MCUXpresso IDE to measure power consumption, perform the following steps:

1. Connect MCU-Link Pro and FRDM-MCXA153 according to Table 9, and then connect MCU-Link Pro and FRDM-MCXA153 to the host personal computer.

Table 9. MCU-Link Pro and FRDM-MCXA153 connection

MCU-Link Pro	FRDM-MCXA153
J9-1	JP2-1
J9-3	JP2-2
J9-2	J3-14

2. Follow the steps in Figure 11 to measure current with MCUXpresso.

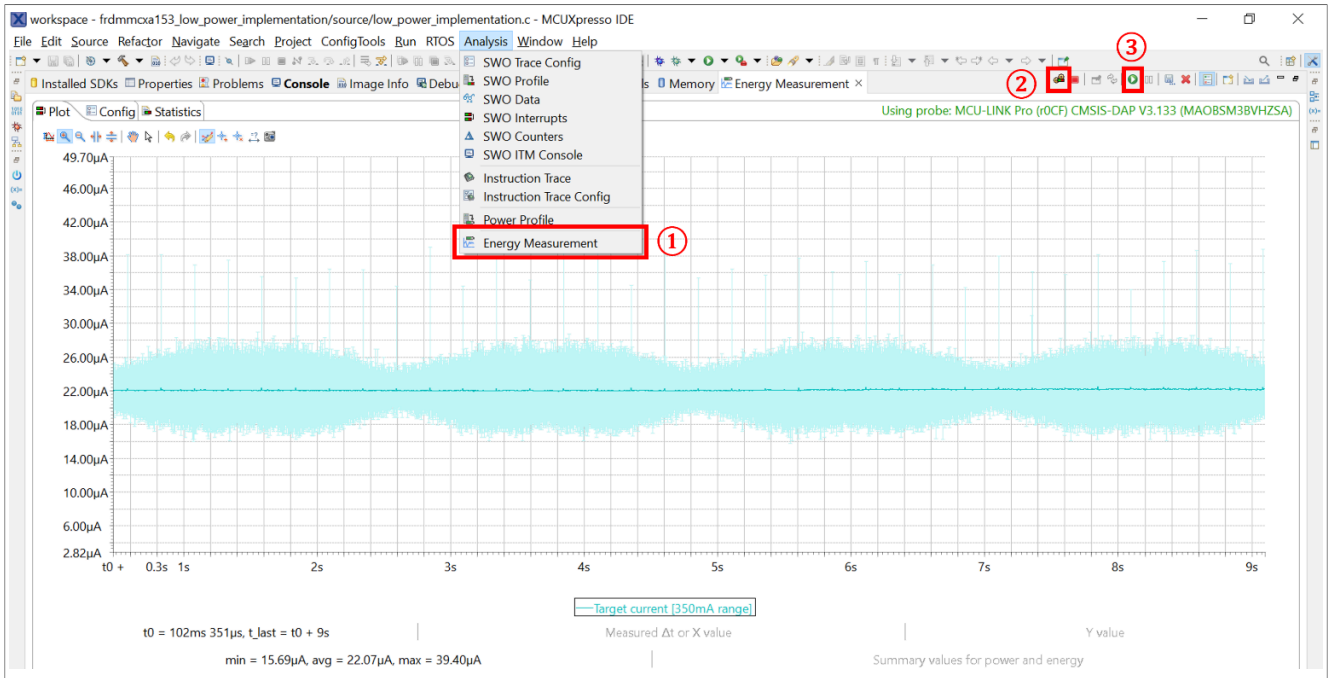

Figure 11. MCUXpresso energy measurement

7.3.5.2 Use multimeter to measure power consumption

You can also use a multimeter to measure the current at JP2 of the FRDM-MCXA153 board.

7.3.6 Measure wake up time

As shown in Figure 12, get the wake up time by measuring the delay between the falling edges of J1-1 (P1_7) and J4-12 (P3_30) using an oscilloscope.

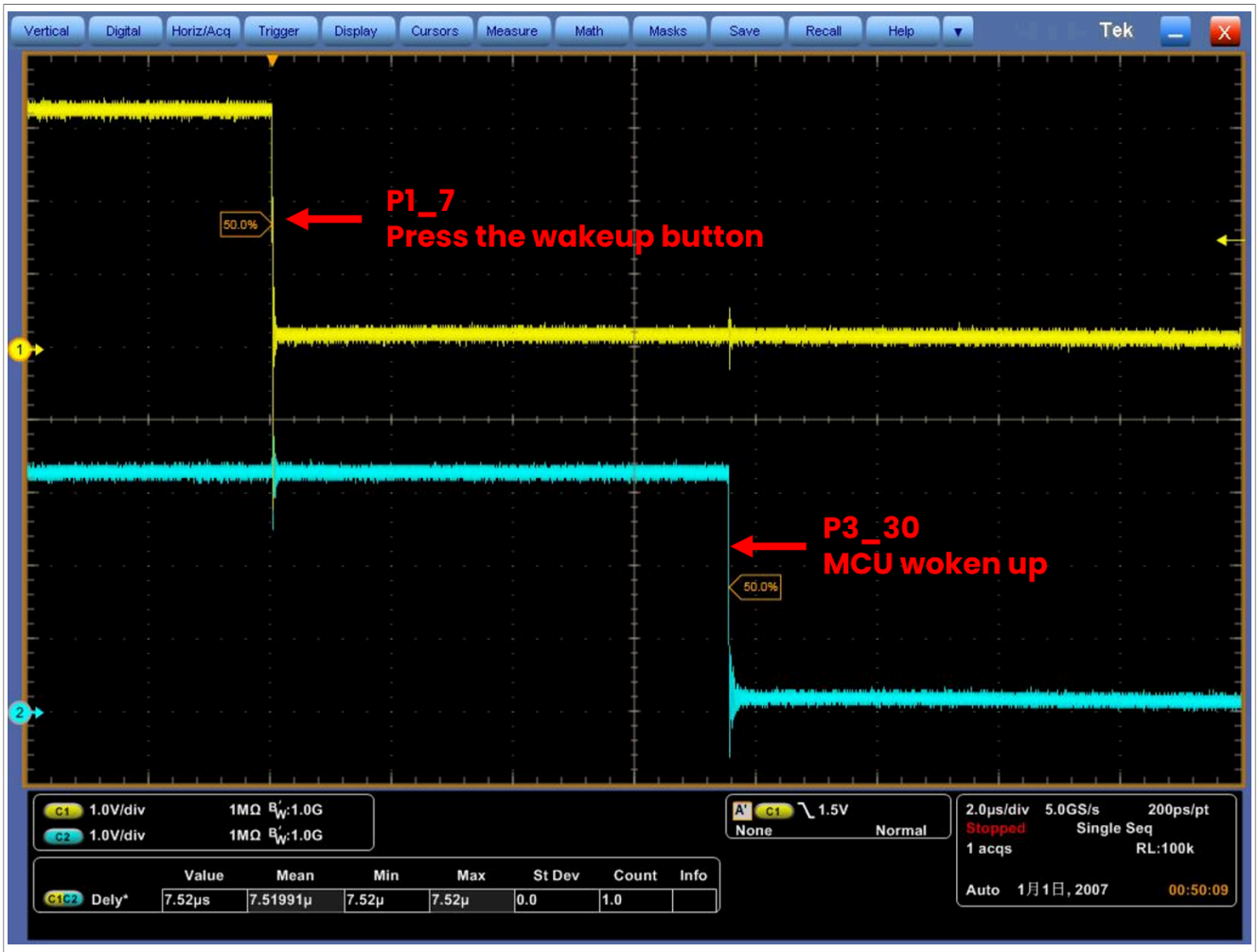

Figure 12. Measure wake up time

7.4 Reference results

Table 10 provides the wake up time and power consumption as a reference.

Note:

- ***P*** *represents the production sample and* ***E*** *represents the engineering sample.*
- *The typical wake up time corresponds to wake up time (**Power mode transition operating behaviors** table) in the data sheet.*
- *Temperature, measuring instrument, and wake up source, and so on, can affect wake up time.*
- *There is no special gate off all peripherals clock, and Deep Power Down mode retained all RAM, so the measured current is a little different from the data in the data sheet.*

Table 10. Reference results

Power mode	Wake up mode	Wake up time (P)	Wake up time (E)	Power consumption (P and E)
Sleep	Typical	0.27 µs	0.27 µs	1.72 mA
Sleep	Fast	0.14 µs	0.14 µs	3.27 mA
Sleep	Slow	1.04 µs	1.04 µs	0.82 mA

Table 10. Reference results*...continued*

Power mode	Wake up mode	Wake up time (P)	Wake up time (E)	Power consumption (P and E)
Deep Sleep	Typical	7.52 µs	4.61 µs	22.1 µA
Deep Sleep	Fast	5.90 µs	2.65 µs	965.2 µA
Deep Sleep	Slow	14.59 µs	11.98 µs	22.0 µA
Power Down	Typical	17.26 µs	13.99 µs	6.2 µA
Power Down	Fast	7.79 µs	4.49 µs	202.8 µA
Power Down	Slow	39.74 µs	36.89 µs	6.2 µA
Deep Power Down	Typical	2.35 ms	2.76 ms	1.1 µA

8 Summary

This application note introduces the power domains, power modes, highlight configurations, wake up, and low power and wake up optimization of MCXA153 series. It provides different low power and wake up configurations through demo for user reference.

9 Note about the source code in the document

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10 Revision history

Table 11 summarizes the revisions to this document.

Table 11. Revision history

Document ID	Release date	Description
AN14558 v1.0	14 February 2025	Initial public release

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